

# DATA SHEET

## **74HC2G86; 74HCT2G86** Dual 2-input exclusive-OR gate

Product specification  
Supersedes data of 2002 Jul 17

2003 Jul 28

## Dual 2-input exclusive-OR gate

## 74HC2G86; 74HCT2G86

## FEATURES

- Wide supply voltage range from 2.0 to 6.0 V
- Symmetrical output impedance
- High noise immunity
- Low power dissipation
- Balanced propagation delays
- Very small 8 pins package
- ESD protection:  
HBM EIA/JESD22-A114-A exceeds 2000 V  
MM EIA/JESD22-A115-A exceeds 200 V.

## DESCRIPTION

The 74HC2G/HCT2G86 is a high-speed Si-gate CMOS device.

The 74HC2G/HCT2G86 provides dual 2-input exclusive-OR gate.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $t_r = t_f \leq 6.0\text{ ns}$ .

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC2G86	HCT2G86	
$t_{PHL}/t_{PLH}$	propagation delay nA to nY	$C_L = 50\text{ pF}$ ; $V_{CC} = 4.5\text{ V}$	11	11	ns
$C_I$	input capacitance		1.5	1.5	pF
$C_{PD}$	power dissipation capacitance per gate	notes 1 and 2	10	9	pF

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in Volts;

$N$  = total switching outputs;

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

2. For 74HC2G86 the condition is  $V_I = \text{GND to } V_{CC}$ .  
For 74HCT2G86 the condition is  $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$ .

## Dual 2-input exclusive-OR gate

74HC2G86; 74HCT2G86

## FUNCTION TABLE

See note 1.

INPUT		OUTPUT
nA	nA	nY
L	L	L
L	H	H
H	L	H
H	H	L

## Note

1. H = HIGH voltage level;  
L = LOW voltage level.

## ORDERING INFORMATION

TYPE NUMBER	PACKAGE					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74HC2G86DP	-40 to +125 °C	8	TSSOP8	plastic	SOT505-2	H86
74HCT2G86DP	-40 to +125 °C	8	TSSOP8	plastic	SOT505-2	T86
74HC2G86DC	-40 to +125 °C	8	VSSOP8	plastic	SOT765-1	H86
74HCT2G86DC	-40 to +125 °C	8	VSSOP8	plastic	SOT765-1	H86

## PINNING

PIN	SYMBOL	DESCRIPTION
1	1A	data input 1A
2	1B	data input 1B
3	2Y	data output 2Y
4	GND	ground (0 V)
5	2A	data input 2A
6	2B	data input 2B
7	1Y	data output 1Y
8	V <sub>CC</sub>	supply voltage

# Dual 2-input exclusive-OR gate

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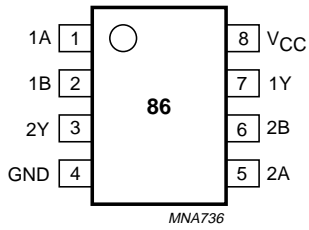


Fig.1 Pin configuration.

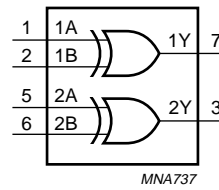


Fig.2 Logic symbol.

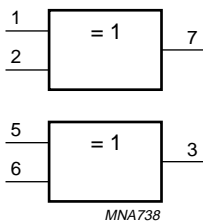


Fig.3 IEC logic symbol.

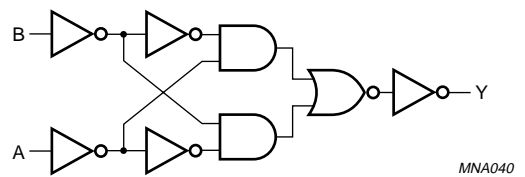


Fig.4 Logic diagram (one driver).

## Dual 2-input exclusive-OR gate

## 74HC2G86; 74HCT2G86

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74HC2G86			74HCT2G86			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
$V_{CC}$	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
$V_I$	input voltage		0	–	$V_{CC}$	0	–	$V_{CC}$	V
$V_O$	output voltage		0	–	$V_{CC}$	0	–	$V_{CC}$	V
$T_{amb}$	operating ambient temperature	see DC and AC characteristics per device	–40	+25	+125	–40	+25	+125	°C
$t_r, t_f$	input rise and fall times	$V_{CC} = 2.0$ V	–	–	1000	–	–	–	ns
		$V_{CC} = 4.5$ V	–	6.0	500	–	6.0	500	ns
		$V_{CC} = 6.0$ V	–	–	400	–	–	–	ns

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	supply voltage		–0.5	+7.0	V
$I_{IK}$	input diode current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V; note 1	–	±20	mA
$I_{OK}$	output diode current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V; note 1	–	±20	mA
$I_O$	output source or sink current	$-0.5$ V < $V_O$ < $V_{CC} + 0.5$ V; note 1	–	25	mA
$I_{CC}$	$V_{CC}$ or GND current	note 1	–	50	mA
$T_{stg}$	storage temperature		–65	+150	°C
$P_D$	power dissipation	$T_{amb} = -40$ to $+125$ °C; note 2	–	300	mW

## Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 110 °C the value of  $P_D$  derates linearly with 8 mW/K.

## Dual 2-input exclusive-OR gate

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## DC CHARACTERISTICS

## Type 74HC2G86

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = 25 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		2.0	1.5	1.2	–	V
			4.5	3.15	2.4	–	V
			6.0	4.2	3.2	–	V
V <sub>IL</sub>	LOW-level input voltage		2.0	–	0.8	0.5	V
			4.5	–	2.1	1.35	V
			6.0	–	2.8	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = –20 µA	2.0	1.9	2.0	–	V
		I <sub>O</sub> = –20 µA	4.5	4.4	4.5	–	V
		I <sub>O</sub> = –20 µA	6.0	5.9	6.0	–	V
		I <sub>O</sub> = –4.0 mA	4.5	4.18	4.32	–	V
		I <sub>O</sub> = –5.2 mA	6.0	5.68	5.81	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 20 µA	2.0	–	0	0.1	V
		I <sub>O</sub> = 20 µA	4.5	–	0	0.1	V
		I <sub>O</sub> = 20 µA	6.0	–	0	0.1	V
		I <sub>O</sub> = 4.0 mA	4.5	–	0.15	0.26	V
		I <sub>O</sub> = 5.2 mA	6.0	–	0.16	0.26	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	6.0	–	–	±0.1	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	6.0	–	–	1.0	µA

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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +85 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		2.0	1.5	–	–	V
			4.5	3.15	–	–	V
			6.0	4.2	–	–	V
V <sub>IL</sub>	LOW-level input voltage		2.0	–	–	0.5	V
			4.5	–	–	1.35	V
			6.0	–	–	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -20 µA	2.0	1.9	–	–	V
		I <sub>O</sub> = -20 µA	4.5	4.4	–	–	V
		I <sub>O</sub> = -20 µA	6.0	5.9	–	–	V
		I <sub>O</sub> = -4.0 mA	4.5	4.13	–	–	V
		I <sub>O</sub> = -5.2 mA	6.0	5.63	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 20 µA	2.0	–	–	0.1	V
		I <sub>O</sub> = 20 µA	4.5	–	–	0.1	V
		I <sub>O</sub> = 20 µA	6.0	–	–	0.1	V
		I <sub>O</sub> = 4.0 mA	4.5	–	–	0.33	V
		I <sub>O</sub> = 5.2 mA	6.0	–	–	0.33	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	6.0	–	–	±1.0	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	6.0	–	–	10	µA

## Dual 2-input exclusive-OR gate

## 74HC2G86; 74HCT2G86

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		2.0	1.5	–	–	V
			4.5	3.15	–	–	V
			6.0	4.2	–	–	V
V <sub>IL</sub>	LOW-level input voltage		2.0	–	–	0.5	V
			4.5	–	–	1.35	V
			6.0	–	–	1.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -20 µA	2.0	1.9	–	–	V
		I <sub>O</sub> = -20 µA	4.5	4.4	–	–	V
		I <sub>O</sub> = -20 µA	6.0	5.9	–	–	V
		I <sub>O</sub> = -4.0 mA	4.5	3.7	–	–	V
		I <sub>O</sub> = -5.2 mA	6.0	5.2	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 20 µA	2.0	–	–	0.1	V
		I <sub>O</sub> = 20 µA	4.5	–	–	0.1	V
		I <sub>O</sub> = 20 µA	6.0	–	–	0.1	V
		I <sub>O</sub> = 4.0 mA	4.5	–	–	0.4	V
		I <sub>O</sub> = 5.2 mA	6.0	–	–	0.4	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	6.0	–	–	±1.0	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	6.0	–	–	20	µA



## Dual 2-input exclusive-OR gate

## 74HC2G86; 74HCT2G86

**Type 74HCT2G86**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = 25 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		4.5 to 5.5	2.0	1.6	–	V
V <sub>IL</sub>	LOW-level input voltage		4.5 to 5.5	–	1.2	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = –20 µA	4.5	4.4	4.5	–	V
		I <sub>O</sub> = –4.0 mA	4.5	4.18	4.32	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 20 µA	4.5	–	0	0.1	V
		I <sub>O</sub> = 4.0 mA	4.5	–	0.15	0.26	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5	–	–	±0.1	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	–	–	1.0	µA
ΔI <sub>CC</sub>	additional supply current per input	V <sub>I</sub> = V <sub>CC</sub> – 2.1 V; I <sub>O</sub> = 0	4.5 to 5.5	–	–	300	µA
<b>T<sub>amb</sub> = –40 to +85 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V <sub>IL</sub>	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = –20 µA	4.5	4.4	–	–	V
		I <sub>O</sub> = –4.0 mA	4.5	4.13	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 20 µA	4.5	–	–	0.1	V
		I <sub>O</sub> = 4.0 mA	4.5	–	–	0.33	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5	–	–	±1.0	µA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	–	–	10	µA
ΔI <sub>CC</sub>	additional supply current per input	V <sub>I</sub> = V <sub>CC</sub> – 2.1 V; I <sub>O</sub> = 0	4.5 to 5.5	–	–	375	µA

## Dual 2-input exclusive-OR gate

## 74HC2G86; 74HCT2G86

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 to +125 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		4.5 to 5.5	2.0	–	–	V
V <sub>IL</sub>	LOW-level input voltage		4.5 to 5.5	–	–	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>					
		I <sub>O</sub> = -20 μA	4.5	4.4	–	–	V
		I <sub>O</sub> = -4.0 mA	4.5	3.7	–	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>					
		I <sub>O</sub> = 20 μA	4.5	–	–	0.1	V
		I <sub>O</sub> = 4.0 mA	4.5	–	–	0.4	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5	–	–	±1.0	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0	5.5	–	–	20	μA
ΔI <sub>CC</sub>	additional supply current per input	V <sub>I</sub> = V <sub>CC</sub> - 2.1 V; I <sub>O</sub> = 0	4.5 to 5.5	–	–	410	μA

## Dual 2-input exclusive-OR gate

## 74HC2G86; 74HCT2G86

## AC CHARACTERISTICS

## Type 74HC2G86

GND = 0 V;  $t_r = t_f \leq 6.0$  ns;  $C_L = 50$  pF.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = 25 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nA, nB to nY	see Figs 5 and 6	2.0	–	34	120	ns
			4.5	–	11	20	ns
			6.0	–	9	17	ns
t <sub>THL</sub> /t <sub>TLH</sub>	output transition time	see Figs 5 and 6	2.0	–	18	75	ns
			4.5	–	6	15	ns
			6.0	–	5	13	ns
<b>T<sub>amb</sub> = –40 to +85 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nA, nB to nY	see Figs 5 and 6	2.0	–	–	150	ns
			4.5	–	–	25	ns
			6.0	–	–	21	ns
t <sub>THL</sub> /t <sub>TLH</sub>	output transition time	see Figs 5 and 6	2.0	–	–	95	ns
			4.5	–	–	19	ns
			6.0	–	–	16	ns
<b>T<sub>amb</sub> = –40 to +125 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nA, nB to nY	see Figs 5 and 6	2.0	–	–	180	ns
			4.5	–	–	36	ns
			6.0	–	–	30	ns
t <sub>THL</sub> /t <sub>TLH</sub>	output transition time	see Figs 5 and 6	2.0	–	–	110	ns
			4.5	–	–	22	ns
			6.0	–	–	20	ns

Dual 2-input exclusive-OR gate

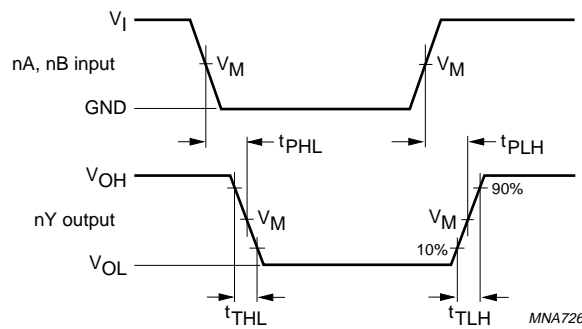
74HC2G86; 74HCT2G86

Type 74HCT2G86

GND = 0 V;  $t_r = t_f \leq 6.0$  ns;  $C_L = 50$  pF.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = 25 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nA, nB to nY	see Figs 5 and 6	4.5	–	11	19	ns
t <sub>THL</sub> /t <sub>TLH</sub>	output transition time	see Figs 5 and 6	4.5	–	6	15	ns
<b>T<sub>amb</sub> = –40 to +85 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nA, nB to nY	see Figs 5 and 6	4.5	–	–	23	ns
t <sub>THL</sub> /t <sub>TLH</sub>	output transition time	see Figs 5 and 6	4.5	–	–	19	ns
<b>T<sub>amb</sub> = –40 to +125 °C</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nA, nB to nY	see Figs 5 and 6	4.5	–	–	48	ns
t <sub>THL</sub> /t <sub>TLH</sub>	output transition time	see Figs 5 and 6	4.5	–	–	22	ns

AC WAVEFORMS

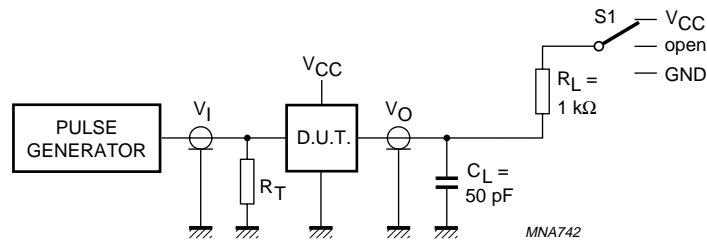


For HC2G:  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
 For HCT2G:  $V_M = 1.3$  V;  $V_I = \text{GND to } 3.0$  V.

Fig.5 The input (nA, nB) to output (nY) propagation delays.

Dual 2-input exclusive-OR gate

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TEST	S1
$t_{PLH}/t_{PHL}$	open
$t_{PLZ}/t_{PZL}$	$V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

Definitions for test circuit:

$R_L$  = Load resistor.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

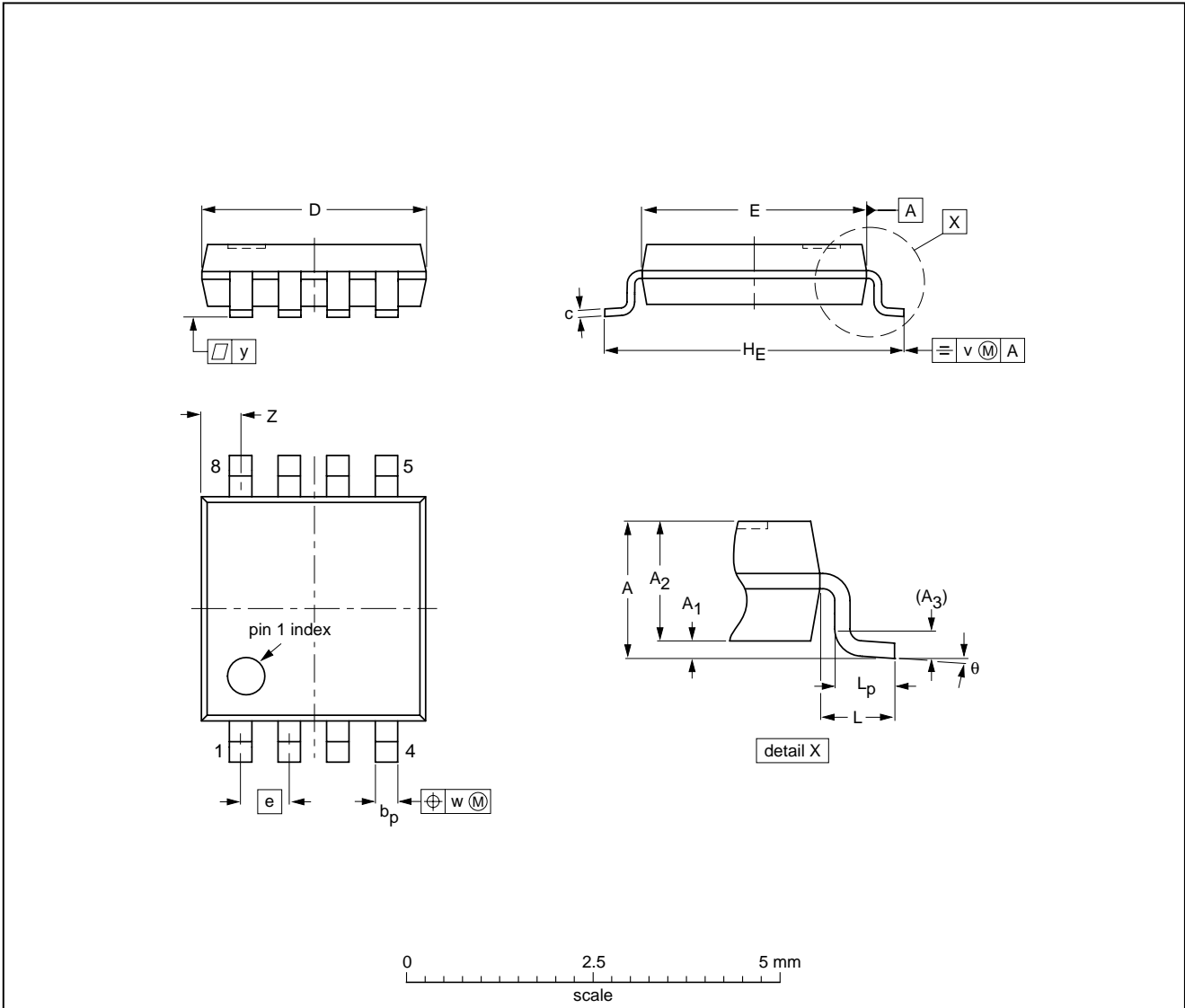
Fig.6 Load circuitry for switching times.

Dual 2-input exclusive-OR gate

74HC2G86; 74HCT2G86

PACKAGE OUTLINES

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	v	w	y	z <sup>(1)</sup>	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

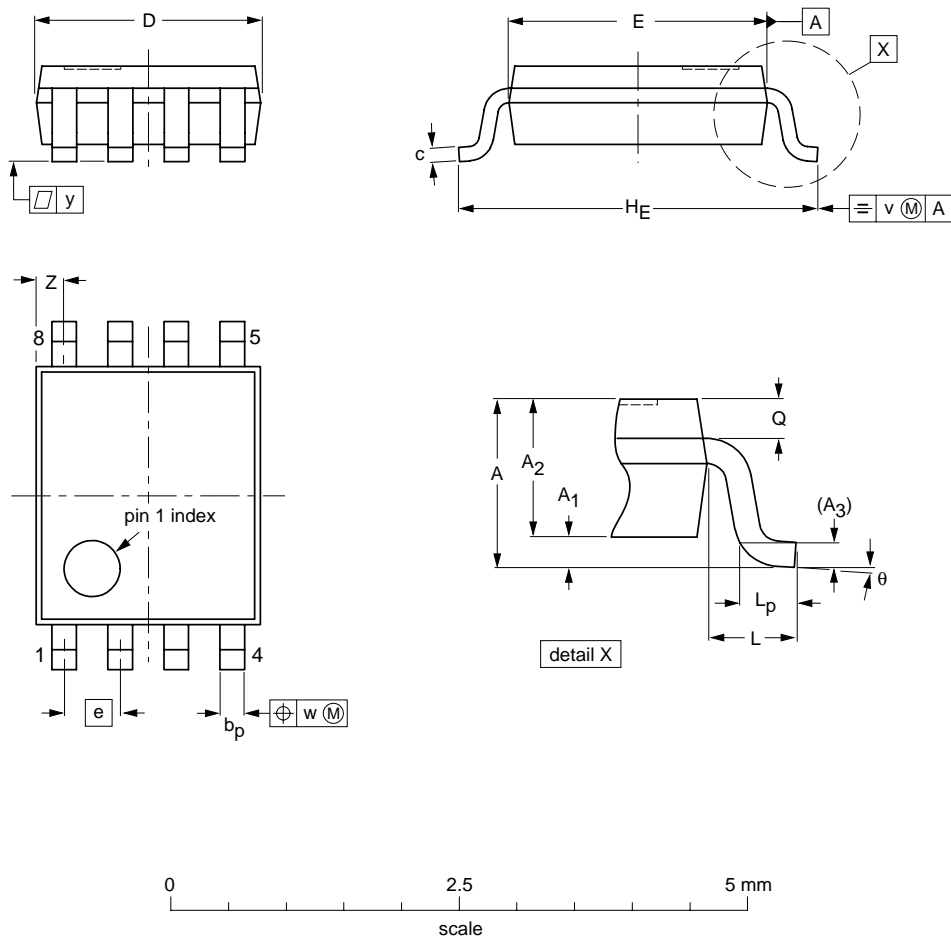
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		---				02-01-16

Dual 2-input exclusive-OR gate

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VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1



**DIMENSIONS** (mm are the original dimensions)

UNIT	A <sub>max.</sub>	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	z <sup>(1)</sup>	θ
mm	1	0.15 0.00	0.85 0.60	0.12	0.27 0.17	0.23 0.08	2.1 1.9	2.4 2.2	0.5	3.2 3.0	0.4	0.40 0.15	0.21 0.19	0.2	0.13	0.1	0.4 0.1	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				02-06-07

## Dual 2-input exclusive-OR gate

## 74HC2G86; 74HCT2G86

## DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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Printed in The Netherlands

613508/02/pp17

Date of release: 2003 Jul 28

Document order number: 9397 750 10567

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